Application of Planar Graph to Design Printed Circuit Board

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***Abstract*—PCB is the realization of electrical circuit that will be used in electronics object. PCB is a 2D board that contain circuit and every component that will be used in electronic network. Electrical circuit can be represented in graph. Then to make 2D board PCB we can utilize the concept of planar graph. This paper is about how to change schematic electrical circuit te become a graph, and prove if it a planar graph so it can be built in PCB, or not. Theories of graph mainly based on Reinhard Diestel book, named "Graph Theory". Euler's Inequality and Kuratowski Theorem can be used to check planarity of graph. The use of planar graphics in PCB manufacturing is intended to make the design process more efficient**

***Keywords*—PCB, Planar Graph, Electronic circuit, design.**

I. About PCB and electrical Circuit

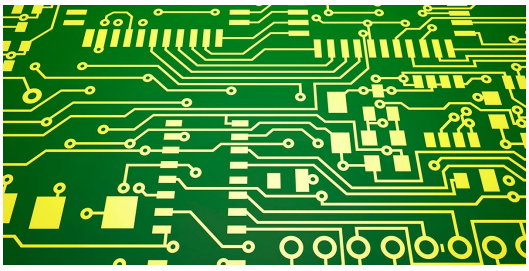


Figure 1. PCB Design that Contain Complex Electrical Circuit

(https://www.techdoze.net/is-a-career-in-pcb-design-worth-it/, accessed on December, 5, 2018 23:40 GMT+7)

PCB (Printed Circuit Board) is a board that is used to connect electronic components with the conductor path layer to form an electronic circuit. Electronic circuit is a series of electronic components arranged into a particular circuit or circuit. Electronic components can include resistors, transistors, voltage sources, diodes, ICs, capacitors, and other electrical components. Each of these electronic components is connected to each other by a certain arrangement, in accordance with the purpose of making the circuit. Each component must be connected to another component, and each component must have the right connection so that the system can produce the appropriate output.

In its realization, to make an electronic circuit initially made a circuit schematic. In an electronic circuit scheme, connections between components must not cut connections between other components. This is because the current flowing will not match the current that is desirable. Thus, this electronic circuit will not produce the appropriate output. In other cases, this intersection can also cause short circuit. The schematic of the electronic circuit will then be realized into a 2D board.

Connections in electronic circuits can be represented as graphs. Each electronic components has node that are vertices of a graph, and the connections that each component has are represented as edges in a graph. Because the electronic circuit will be made into a 2D object, the graph representing the electronic circuit is a planar graph. In manufacturing PCB, the circuit scheme that has been

created will be moved into the PCB design. Each connection that has been made in the circuit schematic, will form a graph on the PCB design. Then the graph will be converted into a planar graph, so that there are no connections between components that intersect the connections between other components, which should not be connected.

II. Theoretical basis

A. Graph

According to "Graph Teory", a book written by Reinhard Diestel, in Chapter 1, graph is a pair G = (V,E) of sets such that E $\subseteq$ $|V|^2$, thus, the elements of E are 2-element subsets of V. The elements of V are the vertices (or nodes, or points) of the graph G, and the elements of E are its edges (or lines). A graph that has no edges called empty graph or null graph.

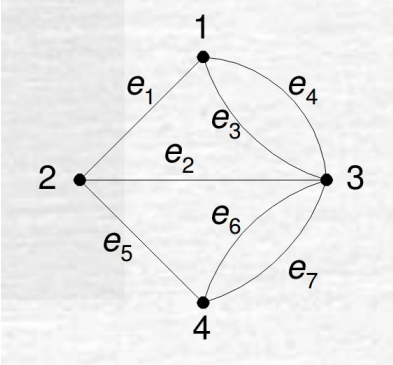


Figure 2. Graph

(http://informatika.stei.itb.ac.id/~rinaldi.munir/Matdis/2015-2016/Graf%20(2015).pdf, accessed on December, 5, 2018 22:40 GMT+7)

For example, in Figure 2, the graph on V = {1, 2, 3, 4} with edge set E = {e1, e2, e3, e4, e5, e6, e7}. In graph, we have some terminologies like adjacent and incident. Two vertices are called adjacent if both of vertices is connected by an edge of graph. In Figure 2, adjacent of 2 are 1, 3, and 4. If all the vertices of graph G are pairwise adjacent, then graph G is complete graph. While, pairwise non-adjacent vertices or edges are called independent or isolated vertex. A vertex v is incident with an edge e if v $\in$ e, then e is an edge at v. For example, in Figure 2 e1 is incident of node 1 and node 2. The two vertices incident with an edge are its end of vertices or ends, and an edge joins its ends.

We can classified graph into 2 based on the presence or absence of a bracelet or double edge on a graph, simple graph and un-simple graph. Simple graph does not contain a bracelet or a double edge while unsimple graph contains a bracelet or a double edge. Moreover, graph can be classified based on direction orientation on its sides too. Undirected graph has no direction orientation. Besides, directed graph or digraph has direction orientation.

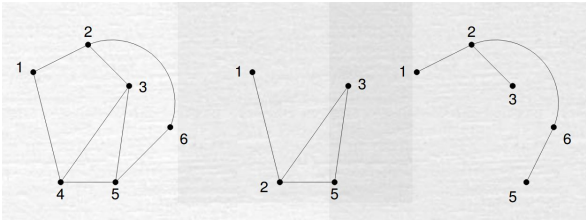


Figure 3. Upagraph and Upagraph Complement

(http://informatika.stei.itb.ac.id/~rinaldi.munir/Matdis/2015-2016/Graf%20(2015).pdf, accessed on December, 5, 2018 23:50 GMT+7)

In the graph there is the term named subgraph and its complement, upagraph complement. Let G = (V, E) a graph. G1 = (V1, E1) is the upgraph (subgraph) of G if V1 $\subseteq$ V and E1 $\subseteq$ E. The complement of the upgraph G1 to graph G is graph G2 = (V2, E2) such that E2 = E - E1 and V2 are sets node that E2 members side by side with.

B. Planar Graph

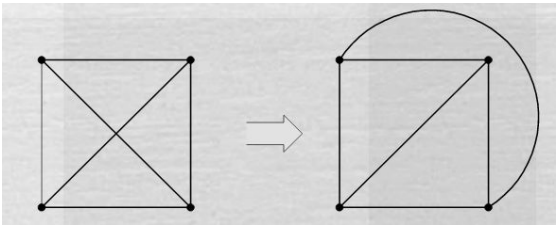


Figure 3. Planar Graph

(http://informatika.stei.itb.ac.id/~rinaldi.munir/Matdis/2015-2016/Graf%20(2015).pdf, accessed on December, 5, 2018 22:40 GMT+7)

Planar graph is a graph that can be drawn on a flat plane with sides that do not intersect (cross other

edges). Euler, a chief mathematician at the Academy at St. Petersburg in 1736, discovered this graph. Besides, plane graph is a pair (V,E) of finite sets with V as set of vertex elements and E as set of edges:

(i) $V \subseteq R^2$

(ii) Every edges is an arc between two vertices

(iii) Different edges have different sets of endpoints

(iv) The interior of an edge contains no vertex and no point of any other edge

Two graphs that seems different in geometry but actually same besides its geometry, called isomorphic graphs. Two graphs, G1 and G2 are said to be isomorphic if there is a one-to-one correspondence between the two vertices and between the sides of both so that the harmony relationship is maintained.

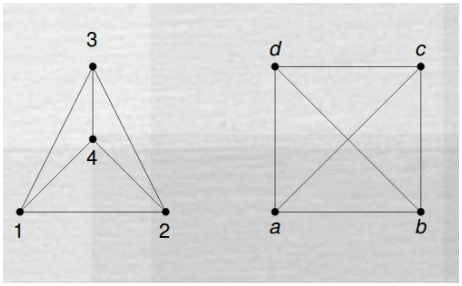


Figure 4. Isomorphic Graph

(http://informatika.stei.itb.ac.id/~rinaldi.munir/Matdis/2015-2016/Graf%20(2015).pdf, accessed on December, 5, 2018 22:40 GMT+7)

As we can see, although both graphs geometrically different, but every nodes is equivalent each other. For example, node 1 equivalent with node a, node 2 equivalent with node b, node 3 equivalent with node c, and node 4 equivalent with node d. Planar graphs that are not plane graphs can be converted into plane graph too because they are isomorphic. So that we can change a graph to be plane graph if the graph is planar graph.

One of the way to find out the planar graph is by using Euler's Inequality. According from reference, Euler's Inequality said that in the form stating, for all triangles inscribed in a given circle, the maximum of the radius of the inscribed circle is reached for the equilateral triangle and only for it, is valid in absolute geometry. For a simple planar graph connected with f regions, n vertices, and e edges ($e > 2$) it always applies:

$$e \leq 3n - 6$$

Planar graph satisfy the inequality. But there some case that don't. For example graph $K_{3,3}$.

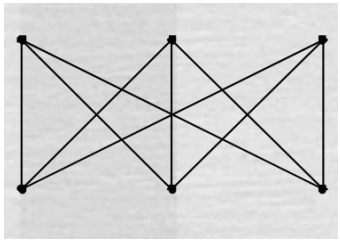


Figure 5. Graph $K_{3,3}$

(http://informatika.stei.itb.ac.id/~rinaldi.munir/Matdis/2015-2016/Graf%20(2015).pdf, accessed on December, 5, 2018 22:40 GMT+7)

$K_{3,3}$ satisfy Euler's Inequality, but $K_{3,3}$ is not planar graph. So, if we derived the formula using new assumption that each area on a planar graph is limited by at least four edges. Then we will get new inequality:

$$e \leq 2n - 4$$

Besides, Euler's Inequality, to check a planar graph, we can use Kuratowski Theorem. Kuratowski Theorem states that graph G is planar if and only if it does not contain isomorphic upagraphs with either Kuratowski or homeomorphic (homeomorphic) graphs with one of the two Kuratowski graph. Here are the properties of Kuratowski graph:

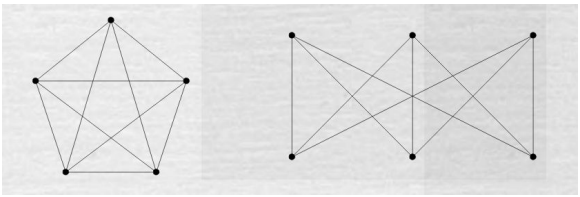
(i) First Kuratowski graph (K_5) and second Kuratowski graph ($K_{3,3}$) are regular graphs.

(ii) Both Kuratowski graphs are non-planar graphs.

(iii) If we remove an edges or vertices of the Kuratowski graph, it become planar graphs.

(iv) The first Kuratowski graphs (K_5) are non-planar graphs with a minimum number of

vertices, while the second Kuratowski graph ($K_{3,3}$) is non-planar graph with a minimum number of sides.



(a) (b)

Figure 6. (a) First Kuratowski Graph (K_5) (b) Second Kuratowski Graph($K_{3,3}$)

(http://informatika.stei.itb.ac.id/~rinaldi.munir/Matdis/2015-2016/Graf%20(2015).pdf, accessed on December, 5, 2018 22:40 GMT+7)

III. Design PCB Using Planar Graph Concept

1. Represented Electrical Circuit in Graph

Electrical circuit contains many component, and the connection between each other depend on complexity of circuit. Well, components of electrical circuit that connected to another component built a node based on circuit and that node can be represented as node in graph. While the connection can be represented as edges of graph.

To design a PCB, we need to built a schematic first to make it easier to design. By making schematic, we will decide which component that is in one node, how we connect each other node, and which component that can't be connected directly. To make schematic from an electrical circuit, I used Altium Designer, one of electrical software that is used to make electrical board, so we can design PCB better. Here is the schematic that we will used to analyze.

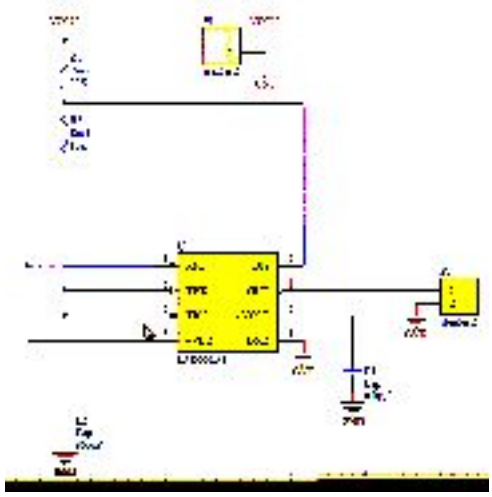


Figure 7. Schematic Electrical Circuit

(https://www.youtube.com/watch?v=9u0Fzpb0yZU, captured and accessed on December, 6, 2018 01:40 GMT+7)

Since we know that every node represented as node in graph, and every connection represented as edge in graph, now we can change the schematic into graph. Beside making node graph from electric nodes, we will make node for every component in electrical circuit too, because here, we assumed every component connected with different connection, although they still in one node. Why we do so, because here, we will design PCB board that will be put up by every component needed. So we must make a node to in every components then nothing will be missed.

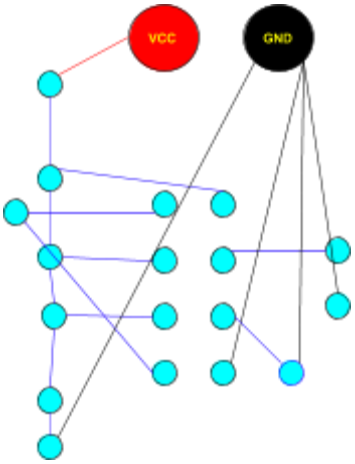


Figure 8. Graph from Electrical Circuit

Since we use Altium Designer that can import schematic electrical circuit into PCB design directly, we can check, if graph that have been made equal to electrical circuit or not.

Figure 9. PCB Design in Altium

(https://www.youtube.com/watch?v=9u0Fzpb0yZU, captured and accessed on December, 6, 2018 01:40 GMT+7)

Although graph in Figure 7 and graph in Figure 9 seems different in geometry, but every node and edges of them is equivalent each other. So since, graph in Figure 8 isomorphic with graph in Figure 9, we can use graph in Figure 8 as reference to do the next step, checking if the graph planar or not.

2. Check Planar Graph Using Euler's Inequality

To check the planarity of graph, we can use Figure 8 to be reference. Because Figure 8 is isomorphic with graph in Figure 9, which is got from schematic, we can set:

$e = 18$

$n = 20$

Then apply Euler's Inequality to find out whether graph of the relevant electrical circuit is planar graph.

$e \leq 3n - 6$

$18 \leq 3 * 20 - 6$

$18 \leq 54$

Because calculation above satisfy Euler's Inequality, we can conclude that graph of electrical circuit that we used, is a planar graph. It means, we can find plane graph from this graph. So now it can be applied in 2D board without mess with jumper after print the PCB. Jumper is used, if we can't find plane graph, because no way to make it 2D.

3. Using Kuratowski Theorem to Check Planar Graph

Although it's been proved that graph in Figure 8 is a planar graph by applying Euler's Inequality. We'll ensure once again using Kuratowski Theorem if graph from this electrical circuits is planar.

Now with Figure 8, we will try to find out if Kuratowski graph is in this graph or not by comparing it, and search if there a subgraph that isomorphic or homomorphic with Kuratowski graph.

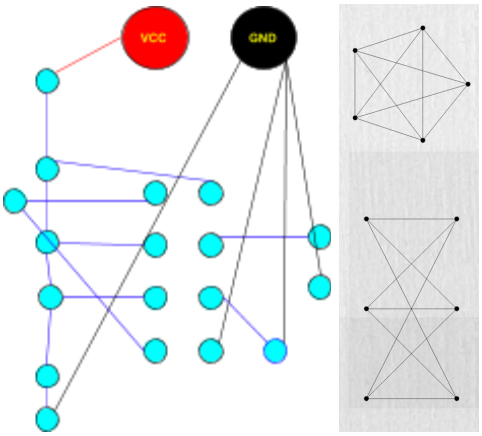


Figure10. Comparison of Graphs with Kuratowski Graphs

As long as we search, still, can't find any subgraph or homograph that isomorphic with Kuratowski graph. It means, we can not prove that this graph is not a planar graph. Instead we can conclude that the graph of this electrical circuit is a planar graph.

4. Modelling to A Planar Graph

As long as we know that the graph given is a planar graph, so we can try to find out a plane graph that isomorphic with this graph. Well, here is one of an isomorphic plane graph from graph of electrical circuit that we used.

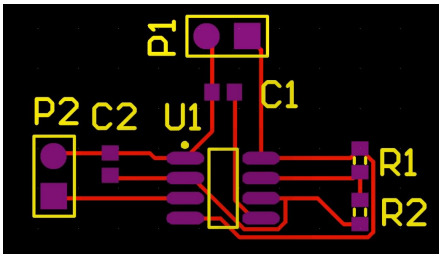


Figure 11. Plan Graph from Electrical Circuit

(https://www.youtube.com/watch?v=9u0Fzpb0yZU, captured and accessed on December, 6, 2018 01:40 GMT+7)

Fortunately, electrical circuit that have been made, produce a planar graph. If it doesn't, we can't really make a 2D PCB board. We need to make a jumper within the connection that intersected. And this think makes it ineffective.

IV. Conclusion

One of way to utilize electrical circuit to built think is trough PCB. Electrical circuit will be printed in PCB and crafted with other electrical components so that the board can be used. To design PCB itself, we need to find a way for all connection between components, so that it won't cross the other connection that must not be crossed each other. Because electrical circuit can be represented in graph, and we want to make this circuit become 2D, we can use planar graph to design PCB easier. This method also can be used to check if initial design and schematic design will produce a planar graph or won't. Applying application of planar graph, will make routing process in PCB designing become easier too.

V. Acknowledgment

The author would like to send her big gratitude to Dr. Rinaldi Muniras, as lecturer of IF2120 for giving the author an opportunity to write this paper and apply the acquired discrete mathematics knowledge to solved case around. The author would also like to thank to them that provide references from variated source, that have been used or cited in this paper so the author can finish this paper with utilizing it to analyze and understanding the problem better.

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Pernyataan

Dengan ini saya menyatakan bahwa makalah yang saya tulis ini adalah tulisan saya sendiri, bukan saduran, atau terjemahan dari makalah orang lain, dan bukan plagiasi.

Bandung, 6 Desember 2019

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