# Graph Theory Applications in Electrical Networks

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***The graph is a traditional way to solve problems with a primitive step-by-step system. So far we have learned that graph theory have solved many problems, one of them is electrical circuits. In electrical circuits, there are many aspects using the graph theory, such as in basic electric circuits into digital computers to Printed Circuit Board (PCB) layout problems.***

***Index Terms*— Bipartite, Electrical circuits, Euler's path, Hamiltonian Cycle, Graph Theory.**

## I. INTRODUCTION

In 1736, Swiss mathematician Leonhard Euler presented a general theory that included a solution to a problem known as the Königsberg bridge problem, a problem that has ignited the thorough study of graph theory until now. Fig. 1(a) shows that a Bandung Institute of Technology satellite map, which is a part of Königsberg. We can see that the GKU Barat are connected to three places; the Indonesia Tenggelam, the Jam Gadang, and the Gerbang Belakang. As seen at thus picture, we can model using a graph as shown in Fig. 1(b). The vertices of the graph represent the locations while the edges represent the pathway connecting the places, the Königsberg bridges.

From the simple mapping, researchers around the world have successfully develop mathematical analyses of graphs, even the engineers nowadays can apply these concepts in their own respective fields.

From now on, the rest of the papers is as follows. Section II presents some important graph terminology. Different graph representations and analysis are discussed in Section III.

## II. GRAPHS TERMINOLOGY AND A BRIEF OF ELECTRICAL CIRCUIT THEOREMS

Graphs basically are discrete structures consisting of vertices and edges that connect these vertices. The vertices, often called nodes in electrical circuits, is usually represented by a circle (either hollow or shaded), and the branch, the analogue of edge in electrical circuits, is represented by a line segment, minimal connecting the two nodes. The graph showed in Fig. 1(b) is called an undirected graph because all od its edges do not indicate any direction from one node to another. However, if the edges of a graph direct one node to another node, as shown in Fig. 2, then the graph is said to be a directed graph.

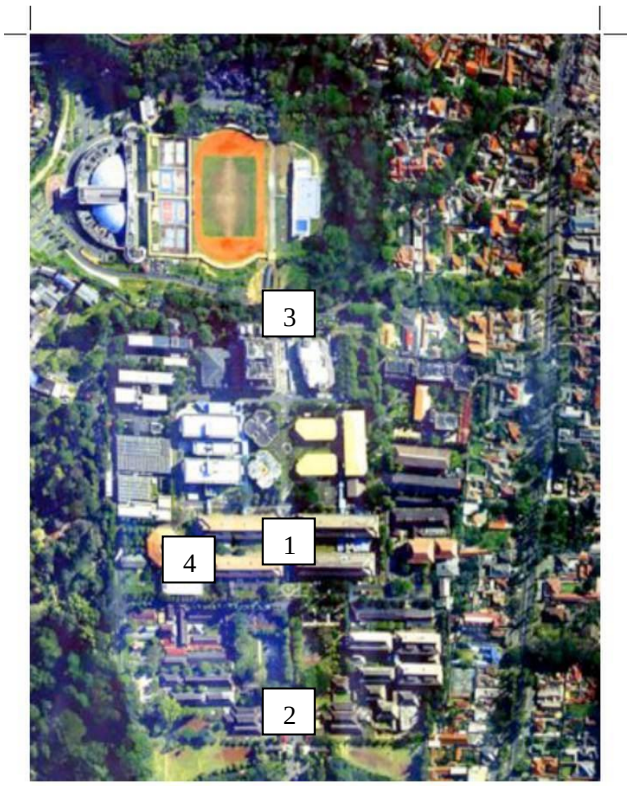
A graph *G* can be mathematically represented by a double *(V,E)*, where V is the set of all vertices, and *E* is the set of all edges. Each edge has either one or two vertices associated with it, called its endpoints. And edge is said to connect its endpoints. If the graph *G(V, E)* is undirected, then each edge e in E is associated with the vertices v and w, and is written as either e = { u, v } or e = { v, u } , i. e. the edge e connects vertices v and w. However, in graph G(V,E) is a directed graph, then each edge e in E is associated with an ordered pair of vertices u and v, and is uniquely written as e = (u,v), i. e. the edge connects vertex u to vertex v, and not the other way around. The association of an edge e to a pair of vertices, for example u and v, means that e is incident on u and v, and u and v are said to be incident on e. Vertice u is said to be adjacent to v, and v is said to be adjacent from u.

Because the edges in graphs with directed edges are ordered pairs, the definition of the degree of a vertex can be refined to reflect the number of edges with this vertex as the initial vertex and as the terminal vertex. In a graph with directed edges the *in-degree of a vertex v*, denoted by $\deg^{-}(v)$, is the number of edges with *v* as their terminal vertex. The *out-degree of v*, denoted by $\deg^{+}(v)$, is the number of edges with *v* as their initial vertex. (Note that a loop at a vertex contributes 1 to both the in-degree and the out-degree of this vertex.) Because each edge has an initial vertex and a terminal vertex, the sum of the in-degrees and the sum of the out-degrees of all vertices in a graph with directed edges are the same. Both of these sums are the number of edges in the graph. This result is stated as Theorem (1).

Let G = ( V, E ) be a graph with directed edges. Then

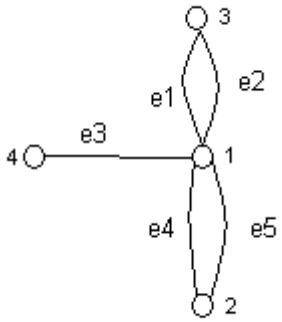
$$\sum_{v \in V} \deg^{-}(v) = \sum_{v \in V} \deg^{+}(v) = |E| \tag{1}$$

Next, the type of the graph is bipartites. A bipartited graph is a graph that each of all edges connect nodes between Vi and Vj. Then the other types are




(Source : http://arieslenterajiwaku.wordpress.com/2012/09/28/peta-itb-ganesha-masa-sekarang/ , Retrieved September 28th 2012)

(a)




(b)

Fig. 1. The Konigsberg problem representation – an example of an undirected graph with four nodes/vertices and five edges. (a). Satellite view of Bandung Institute of Technology, showing paths that connect GKU Barat, the "Jam Gadang", the "Indonesia Tenggelam" and the "Gerbang Belakang".

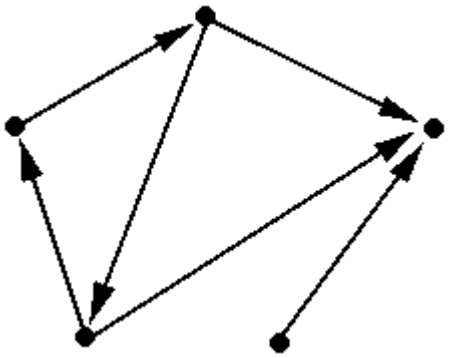


Fig. 2. An example of direct graph with five vertices and six edges.

After a brief of fundamentals of graph theory,these theorems can be applied to a simple electrical circuits. In electrical circuit theory, we can also summing the number of the branch with the following equation

$$b = n + l - 1 \quad (2)$$

Which b represents branch (edge), n for nodes (vertices), and l for loop.

An electrical network is a collection of interconnected electrical elements (or devices) such as resistors, capacitors, inductors, diodes, transistors, vacuum tubes, switches, storage batteries, transformers, delay lines, power sources, and the like. The behavior of an electrical network is a function of two factors : (1) the characteristics of each of the electrical elements, and (2) how they are connected together, that is, their topology. It is the latter factor that brings graph theory into the picture.

## III. Graph Representation

### *A. Matrices*

The graphs are actually can be represented by matrices. The most common used matrices are the adjacency matrix and incidence matrices. The adjacency matrix is a square matrix which each column and row represent edge and vertices.

From the Fig. 1(b), of the Königsberg bridge problem. The graph in Fig. 1(b) has four vertices, $V = \{A,B,C,D\}$. This means that the square matrix must be 4 X 4 , i.e. each row and column is represented by each of the four vertices in $V$. Thus, following Fig. 1(b), the adjacency matrix representing this graph is

$$G_1 = \begin{pmatrix} 0 & 2 & 0 & 0 \\ 2 & 0 & 2 & 1 \\ 0 & 2 & 0 & 0 \\ 0 & 1 & 0 & 0 \end{pmatrix}$$

The way to read is the horizontal and vertical are both correspondents.

### *B. Euler and Hamiltonian Path*

Euler and Hamiltonian paths are two of the most important concepts of graph theory that are applied to the fields of both engineering and sciences. An **Euler path** in a graph $G(V,E)$, which is named after Leonhard Euler (1707-1783), is a path containing every edge of $G(V,E)$. Furthermore, an **Euler circuit** in a graph $G(V,E)$ is a *closed* path containing every edge of $G(V,E)$. In Fig. 1(b), an Euler's path is can be determined as

$$p_x = (4, e_3, 1, e_2, 3, e_1, 1, e_4, 2, e_5, 1) \quad (3)$$

Since ${}_E p$ is a path that contains every edge of $G(V,E)$, it is evident that ${}_E p$ is an Euler path. However, no Euler circuit can be found in Fig. 1(b) since having a closed path would result to having the edge ${}_3 e$ passed more than once.

Having a graph $G(V,E)$ with a large number of vertices and edges will be difficult if an Euler circuit is to be determined. However, there is a theorem that a connected graph has an Euler circuit if and only if each of its vertices has even degree. The **degree** of a vertex is the number of edges incident to it. Looking again at Fig. 1(b), it is seen that the theorem is not satisfied because the degrees of vertices *B* and *D* are both odd, having 5 and 2 incident edges, respectively.

A graph has an Euler path if and only if it has exactly two vertices of odd degree. Fig. 1(b) is an example of graph that has two vertices both having odd degrees, therefore, an Euler path exists.

A **Hamilton path** in a graph $G(V,E)$, which is named after William Rowan Hamilton (1805-1865) is a path containing every vertex of $G(V,E)$. Furthermore, a **Hamilton circuit** in a graph $G(V,E)$ is a *closed* path containing every vertex of $G(V,E)$. Fig. 7 shows an example of a graph that has both a Hamilton path and a Hamilton circuit. An example of a Hamilton path for Fig. 7 is the sequence (1), while an example of a Hamilton circuit for Fig. 7 is the sequence(2).

$$p_x = (A, B, F, C, E, D) \quad (1)$$

$$c_x = (A, B, F, C, E, D, A) \quad (2)$$

If a simple graph $G(V,E)$ with $n \geq 3$ vertices such that the degree of every vertex in $G(V,E)$ is at least $n/2$, then $G(V,E)$ has a Hamilton circuit. This theorem is currently known as the Dirac's theorem. Furthermore, if $G(V,E)$ is a simple graph with $n \geq 3$ vertices such that the sum of the degrees of two nonadjacent vertices is greater than or equal to 3, then $G(V,E)$ has a Hamilton circuit. This theorem is currently known as Ore's theorem.

Paths are practically useful in determining an Euler circuit from a Gray code graph representation. The Gray code, named after Frank Gray, is one of the most useful binary codes in digital systems. One advantage of using Gray code over other binary codes is that only one bit in the code group changes when going from one number to the next. The effect of this method is having minimal errors in transmitting digital signals.

Table 1 presents the four-bit Gray code. Gray codes are commonly used in analog-to-digital signal conversion applications. Gray codes can be represented by a *n* -cube ${}_n Q$ where *n* is the number of bits. A three-bit Gray code can be represented by a 3-cube ${}_3 Q$ as shown in Fig. 10(a), while a four-bit Gray code can be represented by a 4-cube (hypercube) ${}_4 Q$ as shown in Fig. 10(b). Figs. 11(a) and (b) each shows an Euler circuit for ${}_3 Q$ and ${}_4 Q$, respectively.

Another practical application of paths is the optimum fullcustom layout design of a CMOS digital integrated circuit. The idea is to construct a graph representation of the CMOS digital circuit, with the vertices representing the drains and sources of the PMOS and NMOS transistors, and edges representing the transistors themselves. After determining the graph representation of the circuit, all Euler paths are determined and then are used in determining the optimum layout of the circuit.

| Decimal Equivalent | Gray Code | Decimal Equivalent | Gray Code |
|---|---|---|---|
| 0 | 0000 | 8 | 1100 |
| 1 | 0001 | 9 | 1101 |
| 2 | 0011 | 10 | 1111 |
| 3 | 0010 | 11 | 1110 |
| 4 | 0110 | 12 | 1010 |
| 5 | 0111 | 13 | 1011 |
| 6 | 0101 | 14 | 1001 |
| 7 | 0100 | 15 | 1000 |

Table I. 4-bit Gray Code

The Gray code correspondences relations that forms the planar circuit The planar circuits will furthered discussed in section IV.

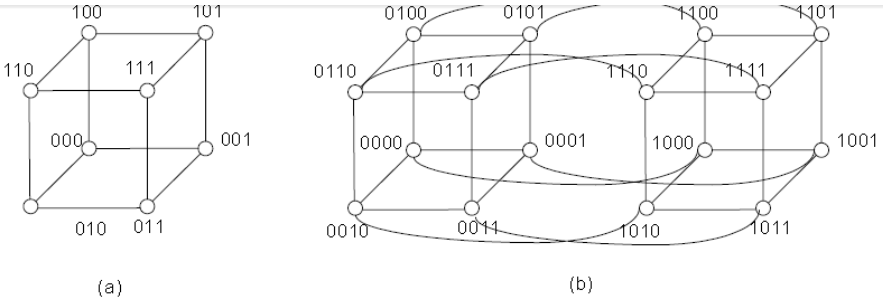
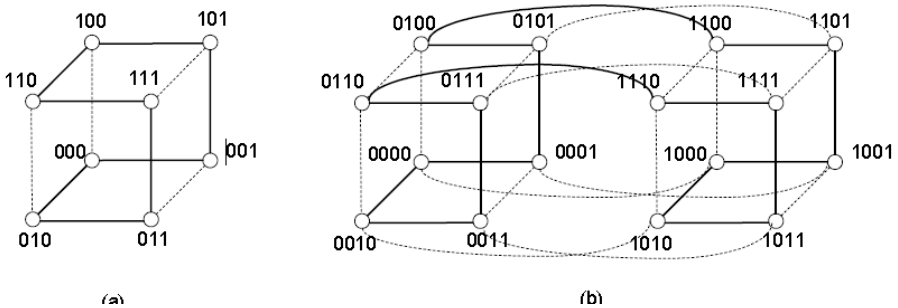



Fig. 10. Graphical representations of Gray codes. (a) $Q_3$. (b) $Q_4$.




### *C. Planar Circuits*

A circuit can be determined as planar circuits if the circuits can be rebuilt in different way without removing a single edge or vertices. This have same concepts as the *isometric graph*, only this is applicated in electrical sciences.

A planar graph is also called a map since the graph is said to "divide the plane" in different regions. In each region of the map, the borders are actually the edges of the planar graph.

There is actually a theorem stating that the sum of the degrees of the regions of a map is twice the number of edges. This theorem is actually called the Euler's Formula and is mathematically stated as

$$V + R = E + 2$$

where V is the number of vertices, R is the number of regions, and E is the number of edges. Another theorem states that $E \leq 3v - 6$ as long as $V \geq 3$.

One typical application of planar graphs is in the design of printed circuit board (PCB) layouts for electric/electronic circuits. Consider, for example, a simple electric circuit shown in Fig. 13 with corresponding graphs shown in Figs. 14(a) and (b). Fig. 14(a) is a straight graphical model of the electric circuit in Fig. 13, with the vertices representing the nodes of the electric circuit, and the edges representing the resistors and wires connected the elements. However, due to the redundancy in the use of nodes, some nodes can be merged to form a single node, thus, minimizing the graph as shown in Fig. 14(b). Since it is obvious that Fig. 14(b) is planar, the PCB electric circuit layout can be designed in such a way that no jumper wires are to be used. The use of the Euler's formula and the other theorems would verify the claim, having $V = 5$, $E = 6$, and $R = 3$, with $V + R = E + 2$ and $E \leq 3V - 6$, $V \geq 3$, being both satisfied.

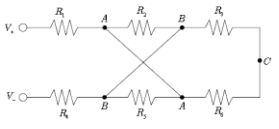


Fig. 13. An example of a simple electric circuit.

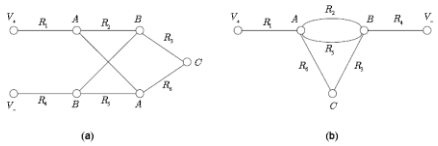


Fig. 14. Graph representations of the simple electric circuit in Fig. 11. (a) A straight graphical representation of Fig. 11. (b) A reduced graphical representation of Fig. 12(a).

## V. CONCLUSION

Graph theory can be used in electronic sciences, because all the electrical circuits and the current are modeled by graphs. There were several analogues in the electronic science term with the graphical theory, one of them is the nodes are analogue with vertices, and the branches are analogue with edges.

The analysis in electrical matters become easier because of the graph theories, as Kirchoff can established his famous laws. He used the directed graphs to describe an electrical circuit, which the directions are the current

pathways. The electrical circuits are only can be determined in connected graphs, because in the disconnected graphs the circuits are open-circuit ( $R = \infty$ ).

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## PERNYATAAN

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Bandung, 30 November 2012

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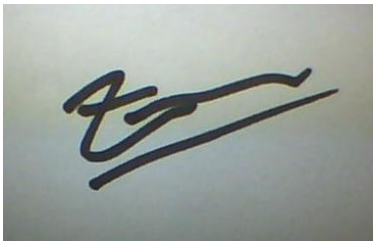

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